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SIMULATION AND PERFORMANCE ANALYSIS OF ELECTRICAL PROPERTIES OF SINGLE GATE AND DOUBLE GATE NANO-MOSFET DEVICES USING FETTOY

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***ABSTRACT**: Nano-scale devices with scale down MOSFET cause problems of high electric fields, high leakage current, heat dissipation, vanishing bulk properties, and shrinkage of depletion regions. In this work, simulation and performance analysis of electrical properties of single gate and double gate nano-MOSFET devices are conducted via FETTOY software. To explore the drain current, quantum capacitance, Gm/Id and quantum capacitance/insulator, the oxide thickness was varied from 1.0 nm to 2.0 nm. The results show that double gate MOSFET device exhibited better performance over single gate, due to its high conductivity and this lead to minimize thermal effect, leakage current and short channel effects.*

***KEYWORDS**: SG-MOSFET, DG- MOSFET, Drain current, FETToy, Oxide thickness,*

INTRODUCTION

Metal-Oxide Semiconductor Field Effect Transistor (MOSFET) is the basic component of microprocessors, memory chips and telecommunications devices. A contemporary microprocessor can accommodate about 2 billion MOSFETs, and a 32-GB memory card [1]. MOSFETs are basically used as switches in logic microcircuits. However, they can be used for many other purposes. The scaling down of the conventional MOSFET in nanoscale range < 100 nm causes a lot of challenges such as short channel effect, high leakage current, heat dissipation, vanishing bulk properties, and shrinkage of depletion regions [2]. To overcome these challenges, many solutions are proposed by different researchers. Some of the solutions include modifications on the conventional structures and technologies aiming to extend their scalability [3]. While other solutions involve the use of new materials and technologies to substitute the conventional silicon MOSFETS[4], transistor miniaturization [5], inserting an electrode on either sides of a DG-MOSFET [6], reduction of gate length and oxide thickness on DG-MOSFET [7], and increasing the gate length of Silicon-on-Insulator (SOI) MOSFET structure [8].To further explore more solutions, in this work, modeling and performance analysis of electrical properties of Single Gate (SG) and Double Gate (DG) -MOSFET devices are conducted via FETTOY 2.0 software. The oxide thickness was varied from 1.0 nm to 2.0 nm and the drain current, quantum capacitance, transconductance, quantum capacitance/insulator are simulated and investigated.

MATETRIALS AND METHOD

This section discussed the materials that are used, simulating software and method of simulation.

2.1. Materials

The materials that are used in this numerical analysis are silicon dioxide used as the gate dielectric, silicon substrate used as base material and the FETToy software as simulating tool freely available on nanohub.org.

2.2. Numerical Simulation

The simulation and analysis of the electrical properties of the SG MOSFET and DG-MOSFET were carried out using FETToy simulating device. FETToy is a set of Matlab scripts that calculate the ballistic I-V characteristics for a conventional SG- MOSFET, DG- MOSFET, Nanowire MOSFETs and Carbon Nanotube MOSFETs [9].The FETTOY Software interface is shown in Figure 1.

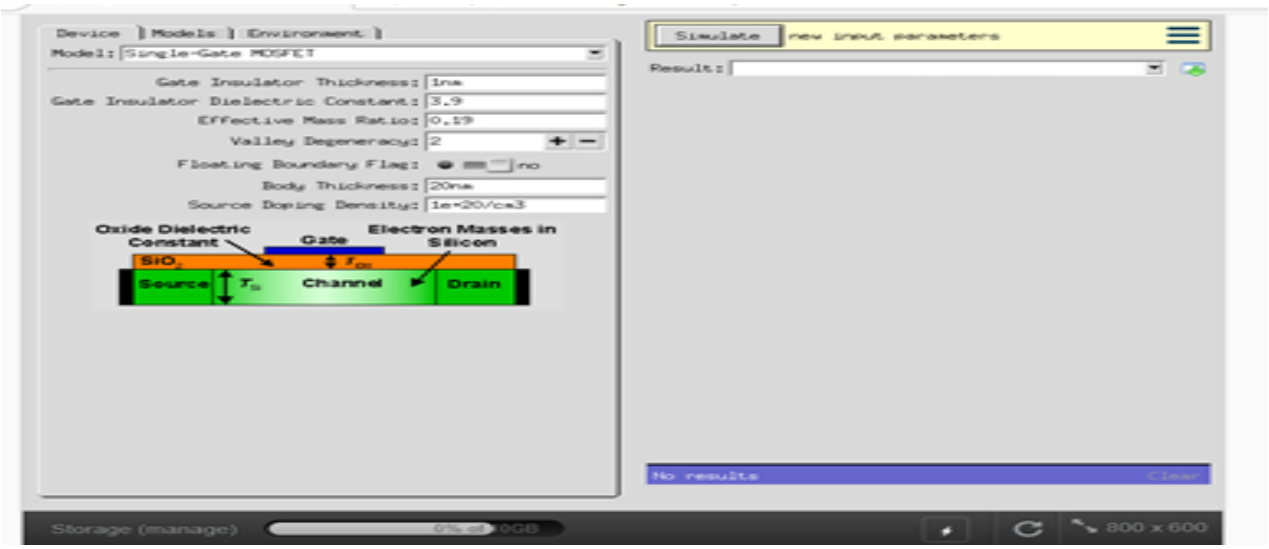

Figure 1: FETTOY Software interface

The design and simulating procedure were as follows;

- Modeling of the device was done by choosing the device type (SG-MOSFET and DG- MOSFET).
- Setting the oxide thickness from 1.0 to 2.0 nm while the remaining input parameters tabularized in Table 1 remain constant.
- The measurement is then stimulated to obtain results for each set of devices chosen.
- Drain current, quantum capacitance, transconductance, quantum capacitance/insulator capacitance and mobile electron results were obtained, displayed and analyzed for both the SG-MOSFET and DG-MOSFET devices.

Table 1: Input parameters used for the simulation

Input Parameters	Value
Oxide thickness (nm)	1.0 – 2.0
Insulator dielectric constant	3.9
Temperature (K)	300
Initial gate voltage (V)	0
Final gate voltage (V)	1
Number of bias points (gate)	13
Initial drain voltage (V)	0
Final drain voltage (V)	1
Number of bias points (drain)	13
Threshold voltage	0.32
Gate control parameter	0.88
Drain control parameter	0.035
Series resistance (Ω)	0
Doping density (cm^{-3})	$1 X 10^{26}$
Si Body thickness (m)	$1 X 10^{-8}$
Transport effective mass	0.19
Valley degeneracy	2

RESULTS AND DISCUSSION

This section presents the results obtained and the discussion of the simulated results.

3.1 Drain Current Characteristics

To determine the drain current at varied oxide thickness, different gate voltage and at a constant drain voltage (1V), the input parameters itemized in Table 1 were used in the FETToy simulation software. Table 2 and Table 3 represent the simulation results obtained for SG-MOSFET and DGMOSFET respectively. While Figure 2 and Figure 3 show the plotted graph of the drain current against gate voltage for both SG-MOSFET and DG-MOSFET at varied oxide thickness. It could be seen from Table 2 and Table 3 that the drain current of double gate nano-MOSFET increases when the oxide thickness decreases from 1.0 nm to 2.0 nm. This indicates that the current capability of DG-MOSFET enhances when the oxide thickness is reduced. It is also observed from the results that the value of the drain current at varied oxide thickness remain steady at a very low gate voltage such as 0V and 0.083V as seen in a similar study reported by [5]. Conclusively, the conductivity of the DG-MOSFET is inversely proportional to the oxide thickness.

Table 2: Drain current against Gate Voltage at different Oxide Thickness in Single Gate MOSFET

Single Gate MOSFET						
At drain voltage 1V						
Gate Voltage (V)	Drain current (uA/um)					
	T_{ox} =1nm	T_{ox} =1.2nm	T_{ox} =1.4nm	T_{ox} =1.6nm	T_{ox} =1.8nm	T_{ox} =2nm
0	0.00685	0.00672	0.00672	0.00672	0.00672	0.00672
0.083333	0.114	0.114	0.114	0.114	0.114	0.114
0.166666	1.92	1.91	1.9	1.9	1.89	1.89
0.25	27.2	25.5	24.7	24	23.4	22.7
0.333333	169	140	128	119	111	104
0.416666	455	351	312	282	257	237
0.5	846	628	550	489	441	401
0.583333	1330	960	830	732	654	591
0.666666	1880	1340	1150	1010	893	803
0.75	2510	1760	1500	1310	1160	1040
0.833333	3220	2220	1890	1630	1440	1290
0.916666	3990	2730	2310	1990	1750	1550
1	4820	3290	2760	2370	2070	1840

Table 3: Drain current against Gate Voltage at different Oxide Thicknesses in Double Gate MOSFET

Double Gate MOSFET						
At drain voltage 1V						
Gate Voltage (V)	Drain current (uA/um)					
	T_{ox}=1nm	T_{ox} =1.2nm	T_{ox} =1.4nm	T_{ox} =1.6nm	T_{ox} =1.8nm	T_{ox} =2nm
0	0.0672	0.0672	0.0672	0.00672	0.0672	0.00672
0.083333	0.114	0.114	0.114	0.114	0.114	0.114
0.166666	1.93	1.93	1.92	1.92	1.92	1.92
0.25	28.9	28.3	27.8	27.3	26.8	26.4
0.333333	213	197	183	172	162	154
0.416666	647	575	517	471	433	401
0.5	1280	1120	988	886	803	735
0.583333	2090	1790	1570	1390	1250	1140
0.666666	3050	2590	2250	1980	1770	1600
0.75	4150	3510	3030	2660	2360	2120
0.833333	5360	4530	3900	3410	3020	2700
0.916666	6680	5640	4850	4230	3740	3340
1	8090	6830	5860	5110	4510	4030

It has been discovered from Table 2 and Table 3 that the drain current of double gate Nano-MOSFET increases with the reduction in oxide thickness. It means that when reducing the oxide thickness, the current capability of double gate Nano-MOSFET enhances. It is also discovered from the simulation that at a very low gate voltage such as 0V and 0.083V, the value of drain current is the same for all oxide thickness investigated. A graph of drain current against gate voltage was plotted for both single gate and double gate Nano-MOSFET for all oxide thickness (1nm, 1.2nm, 1.4nm, 1.6nm, 1.8nm and 2nm) as shown in Fig.6 and Fig.7. This is in agreement with the study reported by [5]. I can wrap up that the conductivity of the double gate Nano-MOSFET is inversely proportional to the oxide thickness.

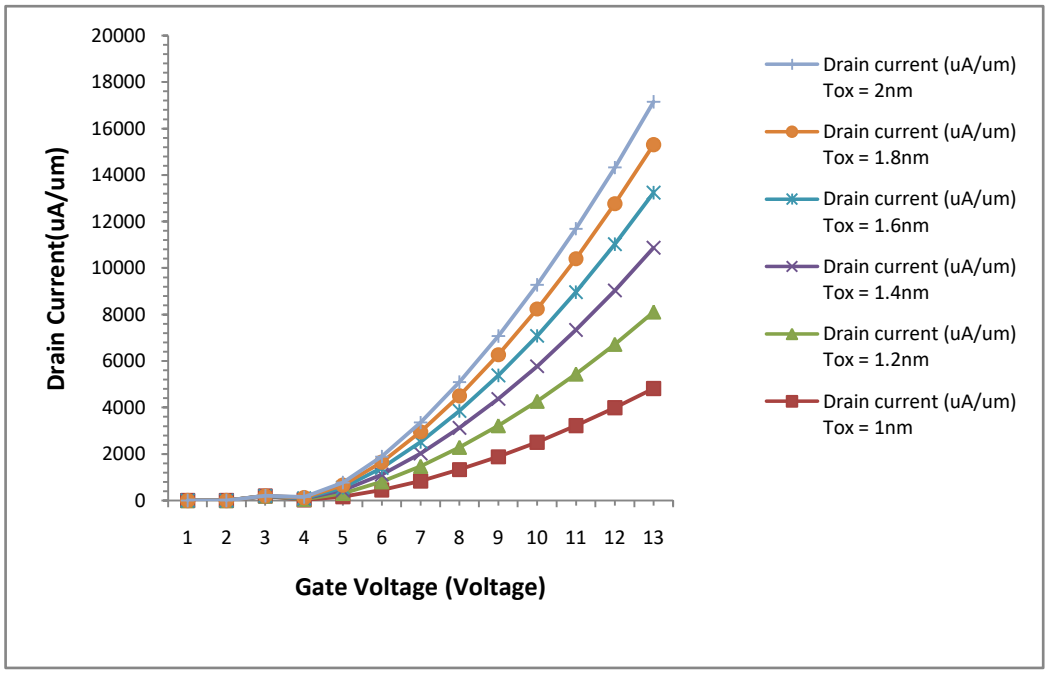

Figure 6: Graph of drain current against gate voltage for different oxide thicknesses in single gate MOSFET

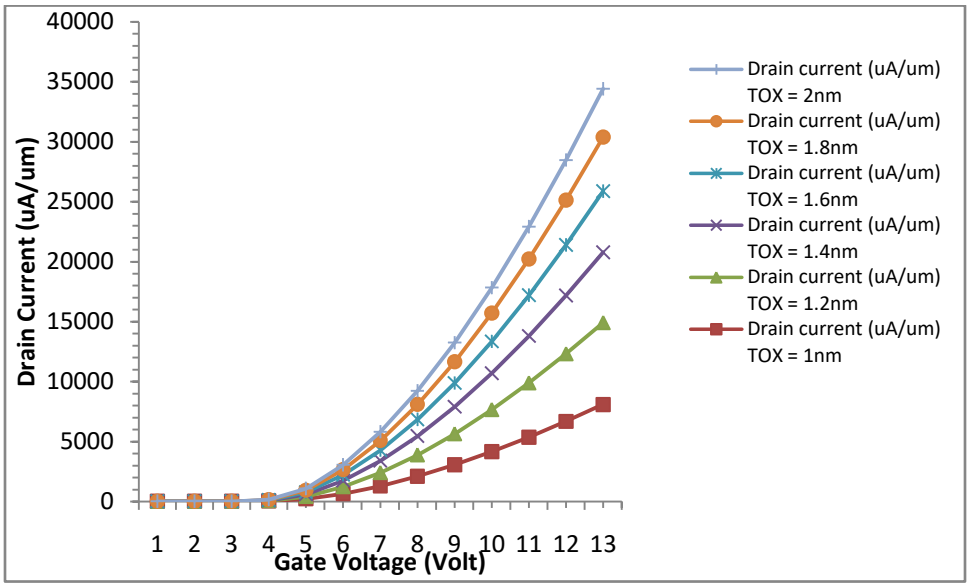

Figure 7: Graph of drain current against gate voltage for different oxide thicknesses in double gate MOSFET

3.2 Quantum Capacitance Characteristics

Table 4 and Table 5 shows the simulation results of single gate and double gate Nano-MOSFET independently for input parameter given in Table 1, in determining the quantum capacitance at different gate voltage, oxide thickness and at a constant drain voltage of 1V.

Table 4: Quantum capacitance against Gate Voltage at different Oxide Thicknesses in Single Gate MOSFET

Single Gate MOSFET						
At drain voltage 1V						
Gate Voltage (V)	Quantum Capacitance (F/cm^2)					
	Tox=1nm	Tox=1.2nm	Tox=1.4nm	Tox=1.6nm	Tox=1.8nm	Tox=2nm
0	2.1e-10	2.1e-10	2.1e-10	1.2e-10	2.1e-10	2.1e-10
0.083333	3.58e-09	3.57e-09	3.57e09	3.57e-09	3.57e-09	3.57e-09
0.166666	5.97e-08	5.95e-08	5.94e-08	5.92e-08	5.9e-08	5.88e-08
0.25	7.9e-07	7.65e-07	7.43e-07	7.22e-07	7.03e-07	6.85e-07
0.333333	3.84e-06	3.56e-06	3.32e-06	3.11e-06	2.94e-06	2.78e-06
0.416666	7.42e-06	6.86e-06	6.38e-06	5.98e-06	5.62e-06	5.31e-06
0.5	9.84e-06	9.25e-06	8.72e-06	8.24e-06	7.81e-06	7.42e-06
0.583333	1.12e-05	1.07e-05	1.03e-05	9.82e-06	9.4e-06	9.01e-06
0.666666	1.2e-05	1.16e-05	1.12e-05	1.09e-05	1.05e-05	1.02e-05
0.75	1.24e-05	1.21e-05	1.18e-05	1.16e-05	1.13e-05	1.1e-05
0.833333	1.26e-05	1.24e-05	1.22e-05	1.2e-05	1.18e-05	1.15e-05
0.916666	1.27e-05	1.26e-05	1.24e-05	1.23e-05	1.21e-05	1.19e-05
1	1.27e-05	1.27e-05	1.26e-05	1.25e-05	1.23e-05	1.22e-05

Table 5: Quantum capacitance against Gate Voltage at different Oxide Thicknesses in Double Gate MOSFET

Double Gate MOSFET						
At drain voltage 1V						
Gate Voltage (V)	Quantum Capacitance (F/cm2)					
	Tox=1nm	Tox=1.2nm	Tox=1.4nm	Tox=1.6nm	Tox=1.8nm	Tox=2nm
0	2.1e-10	2.1e-10	2.1e-10	2.1e-10	2.1e-10	2.1e-10
0.083333	3.58e-09	3.58e-09	3.58e-09	3.58e-09	3.58e-09	3.58e-09
0.166666	6.02e-08	6.01e-08	6e-08	5.99e-08	5.98e-08	5.97e-08
0.25	8.62e-07	8.46e-07	8.31w-07	8.17e-07	8.03e-07	7.9e-07
0.333333	4.92e-06	4.64e-06	4.41e-06	4.2e-06	4.01e-06	3.84e-06
0.416666	9.36e-06	8.89e-06	8.47e-06	8.09e-06	7.74e-06	7.42e-06
0.5	1.15e-05	1.12e-05	1.08e-05	1.05e-05	1.02e-05	9.84e-06
0.583333	1.23e-05	1.21e-05	1.19e-05	1.17e-05	1.15e-05	1.12e-06
0.666666	1.26e-05	1.25e-05	1.24e-05	1.23e-05	1.21e-05	1.2e-05
0.75	1.27e-05	1.27e-05	1.26e-05	1.26e-05	1.25e-06	1.24e-05
0.833333	1.28e-05	1.28e-05	1.27e-05	1.27e-05	1.26e-05	1.26e-05
0.916666	1.28e-05	1.28e-05	1.28e-05	1.27e-05	1.27e-05	1.27e-05
1	1.28e-05	1.28e-05	1.28e-05	1.28e-05	1.27e-05	1.27e-05

It has been discovered from Table 4 and Table 5 that the quantum capacitance (QC) of both single gate and double gate Nano-MOSFET increases significantly as the oxide thickness goes down from 2nm to 1nm, and gate voltage increases. It is also discovered from the simulation that at a very low gate voltage such as 0V and 0.083V, the value of quantum capacitance is the same for all oxide thickness investigated here. A graph of quantum capacitance against gate voltage was plotted for both single gate and double gate Nano-MOSFET for all oxide thickness (1nm, 1.2nm, 1.4nm, 1.6nm 1.8nm and 2nm) as shown in Fig.8 and Fig.9. For single gate MOSFET, I can easily wrap up that with decrease in oxide thickness the quantum capacitance increases at different gate voltages. Whereas, in the case of double gate MOSFET under identical simulating condition the decrease in gate oxide thickness the quantum capacitance increases at different gate voltages.

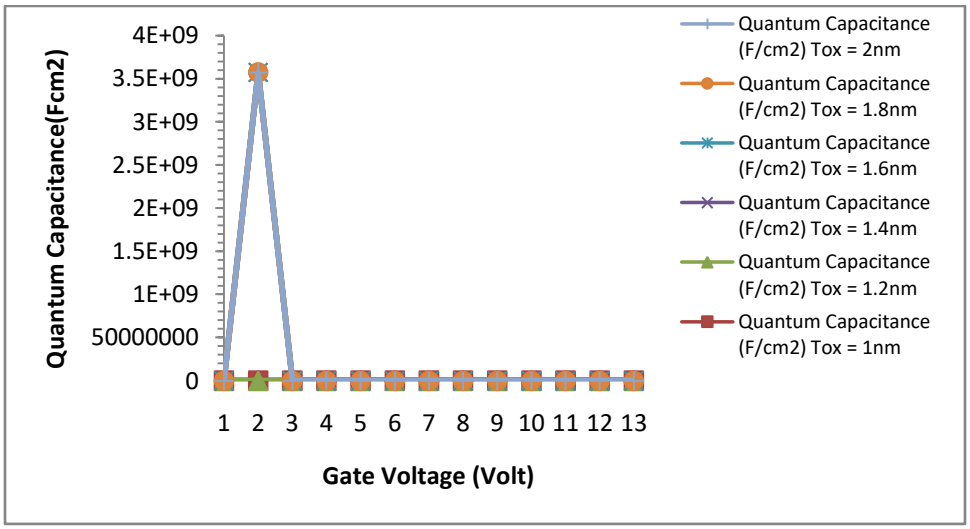

Figure 8: Graph of quantum capacitance against gate voltage for different oxide thicknesses in single gate MOSFET

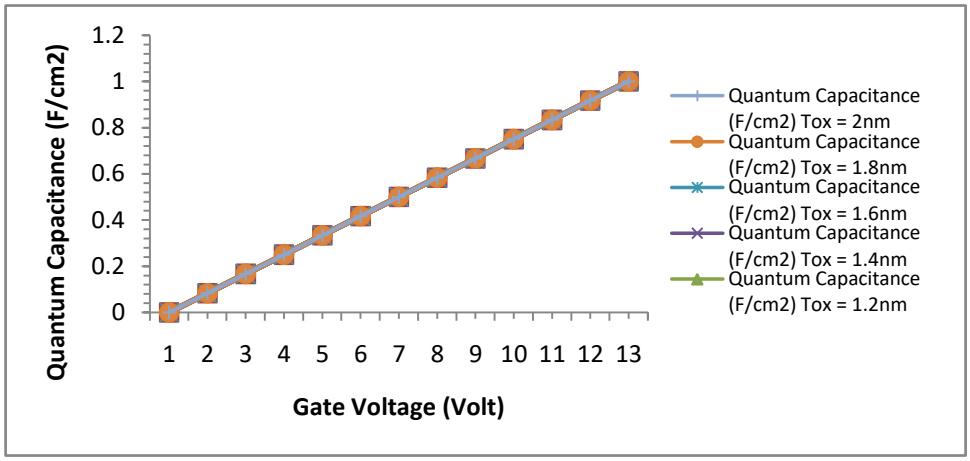

Figure 9: Graph of quantum capacitance against gate voltage for different oxide thicknesses in double gate MOSFET.

3.3 Gm /Id Ratio Characteristics

Table 6 and Table 7 shows the simulation results of single gate and double gate Nano-MOSFET independently for input parameter given in Table 1, in determining the Gm /Id at different gate voltage, oxide thickness and at a constant, drain voltage of 1V.

Table 6: Gm /Id against Gate Voltage at different Oxide Thicknesses in Single Gate MOSFET

Single Gate MOSFET						
At drain voltage 1V						
Gate Voltage (V)	Gm/id					
	T_{ox}=1nm	T_{ox} =1.2nm	T_{ox}=1.4nm	T_{ox}=1.6nm	T_{ox}=1.8nm	T_{ox}=2nm
0	34	34	34	34	34	34
0.083333	33.9	33.9	33.9	33.9	33.8	33.8
0.166666	32.6	32.5	32.3	32.1	31.9	31.8
0.25	26.3	25.7	25.3	24.8	24.4	24
0.333333	16.3	15.7	15.2	14.8	14.4	14.1
0.416666	9.38	9.03	8.74	8.5	8.29	8.11
0.5	6.25	6.05	5.87	5.73	5.6	5.49
0.583333	4.67	4.54	4.42	4.32	4.24	4.16
0.666666	3.74	3.63	3.55	3.48	3.42	3.36
0.75	3.14	3.05	2.97	2.92	2.86	2.82
0.833333	2.72	2.65	2.58	2.52	2.47	2.44
0.916666	2.4	2.34	2.29	2.23	2.19	2.15
1	2.25	2.21	2.16	2.11	2.07	2.03

Table 7: Gm/Id against Gate Voltage at different Oxide Thicknesses in Double Gate MOSFET

Double Gate MOSFET						
At drain voltage 1V						
Gate Voltage (V)	Gm/id					
	T_{ox}=1nm	T_{ox}=1.2nm	T_{ox}=1.4nm	T_{ox}=1.6nm	T_{ox}=1.8nm	T_{ox}=2nm
0	34	34	34	34	34	34
0.083333	34	34	33.9	33.9	33.9	33.9
0.166666	33.2	33.1	33	32.9	32.8	32.6
0.25	28.2	27.8	27.3	27	26.6	26.3
0.333333	18.7	18.1	17.5	17.1	16.7	16.3
0.416666	10.8	10.4	10.1	9.83	9.59	9.38
0.5	7.02	6.82	6.65	6.5	6.37	6.25
0.583333	5.18	5.04	4.93	4.83	4.74	4.67
0.666666	4.12	4.04	3.95	3.87	3.8	3.74
0.75	3.4	3.36	3.31	3.25	3.2	3.14
0.833333	2.86	2.85	2.82	2.8	2.76	2.72
0.916666	2.46	2.46	2.45	2.44	2.42	2.4
1	2.3	2.29	2.28	2.27	2.26	2.25

It has been discovered from Table 6 and Table 7 that the Gm/Id ratio of both single gate and double gate Nano-MOSFET increases significantly as the oxide thickness goes down from 2nm to 1nm, and gate voltage increases this is due to the reason that gate oxide capacitance is increased as the gate insulator thickness is reduced. It is also discovered from the simulation that at a very low gate voltage such as 0V and 0.083V, the value of Gm/Id ratio is the same for all oxide thickness investigated. A graph of Gm/Id ratio against gate voltage was plotted for both single gate and double gate Nano-MOSFET for all oxide thickness (1nm, 1.2nm, 1.4nm, 1.6nm, 1.8nm and 2nm) as shown in Fig.10 and Fig.11.

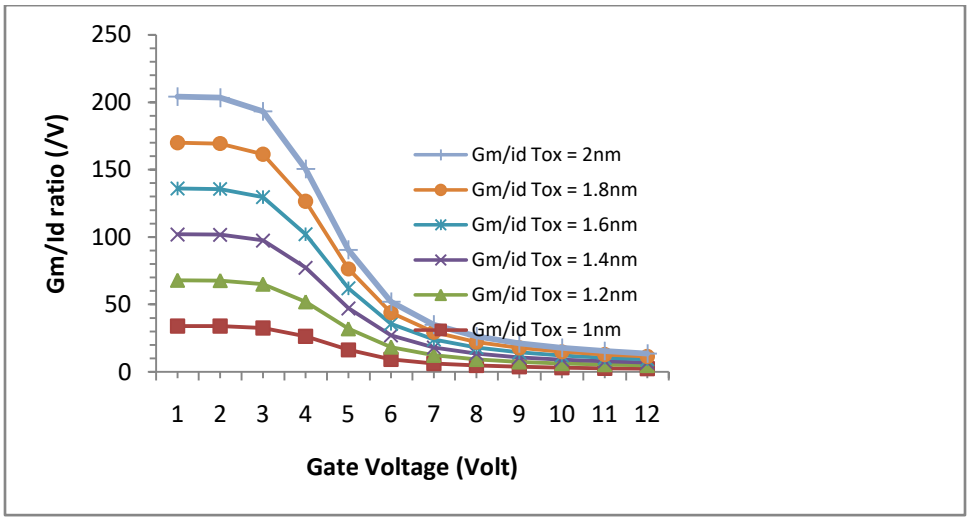

Figure 10: Graph of Gm/Id ratio against gate voltage for different oxide thicknesses in single gate MOSFET

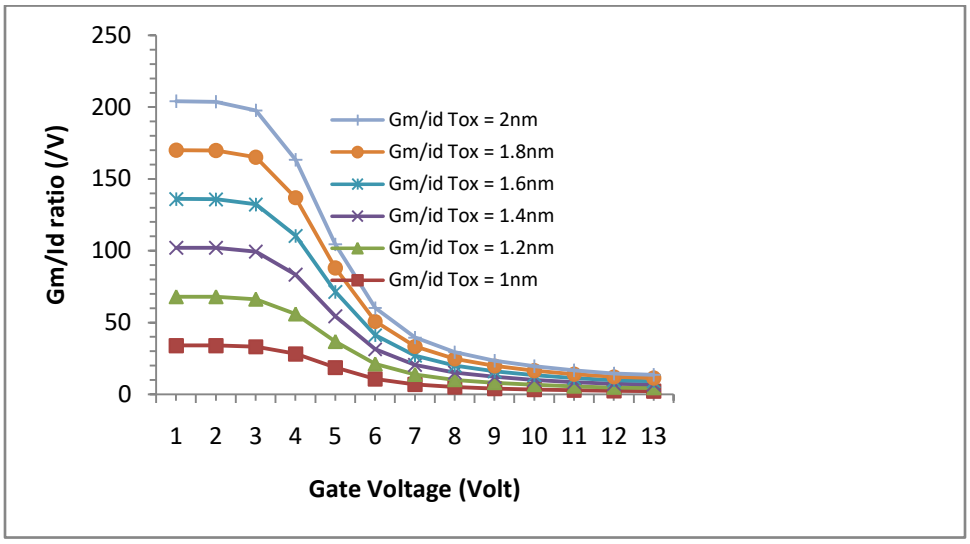

Figure 11: Graph of Gm/Id ratio against gate voltage for different oxide thicknesses in double gate MOSFET

3.4 QC/Insulator capacitance ratio Characteristics

Table 8 and Table 9 shows the simulation results of single gate and double gate Nano-MOSFET independently for input parameter given in Table 1, in determining the QC/Insulator capacitance ratio at different gate voltage, oxide thickness and at a constant drain voltage of 1V.

Table 8: QC/ Insulator Capacitance against Gate Voltage at different Oxide Thicknesses in Single Gate MOSFET

Single Gate MOSFET						
At drain voltage 1V						
Gate Voltage (V)	Quantum Capacitance/Insulator Capacitance					
	T_{ox}=1nm	T_{ox}=1.2nm	T_{ox}=1.4nm	T_{ox} =1.6nm	T_{ox} =1.8nm	T_{ox} = 2nm
0	6.09e-05	7.31e-05	8.53e-05	9.75e-05	0.00011	0.000122
0.083333	0.00104	0.00124	0.00145	0.00166	0.00186	0.00207
0.166666	0.0173	0.0207	0.0241	0.0274	0.0308	0.0341
0.25	0.229	0.266	0.301	0.335	0.367	0.397
0.333333	1.11	1.24	1.35	1.44	1.53	1.61
0.416666	2.15	2.38	2.59	2.77	2.93	3.38
0.5	2.85	3.22	3.54	3.82	4.07	4.3
0.583333	3.25	3.73	4.16	4.55	4.9	5.22
0.666666	3.47	4.04	4.56	5.04	5.48	5.88
0.75	3.58	4.21	4.81	5.36	5.87	6.35
0.833333	3.64	4.31	4.96	5.56	6.14	6.68
0.916666	3.67	4.37	5.05	5.69	6.31	6.9
1	3.69	4.4	5.1	5.78	6.43	7.06

Table 9: QC/ Insulator Capacitance against Gate Voltage at different Oxide Thicknesses in Double Gate MOSFET

Double Gate MOSFET						
At drain voltage 1V						
Gate Voltage (V)	Quantum Capacitance/ Insulator Capacitance					
	T_{ox}=1nm	T_{ox}=1.2nm	T_{ox}=1.4nm	T_{ox}=1.6nm	T_{ox}=1.8nm	T_{ox} = 2nm
0	6.09e-05	7.31e-05	8.53e-05	9.75e-05	0.00011	0.000122
0.083333	0.00104	0.00124	0.00145	0.00166	0.00186	0.00207
0.166666	0.0174	0.0209	0.0243	0.0278	0.0312	0.0346
0.25	0.25	0.294	0.337	0.379	0.419	0.458
0.333333	1.42	1.61	1.79	1.95	2.09	2.23
0.416666	2.71	3.09	3.44	3.75	4.04	4.3
0.5	3.34	3.88	4.39	4.86	5.29	5.7
0.583333	3.58	4.22	4.84	5.42	5.98	6.5
0.666666	3.66	4.36	5.04	5.69	6.33	6.93
0.75	3.69	4.41	5.12	5.82	6.5	7.16
0.833333	3.7	4.43	5.16	5.88	6.58	7.28
0.916666	3.7	4.44	5.17	5.9	6.63	7.34
1	3.7	4.44	5.18	5.91	6.65	7.37

It has been discovered from Table 8 and Table 9 that the QC/Insulator capacitance ratio of both single gate and double gate Nano-MOSFET decreases as the oxide thickness goes down from 2nm to 1nm, and gate voltage increases. Lower drain voltage shows significant capacitance effect. It is also discovered from the simulation that at a very low gate voltage such as 0V, the value of QC/Insulator capacitance ratio is the same for all oxide thickness investigated.

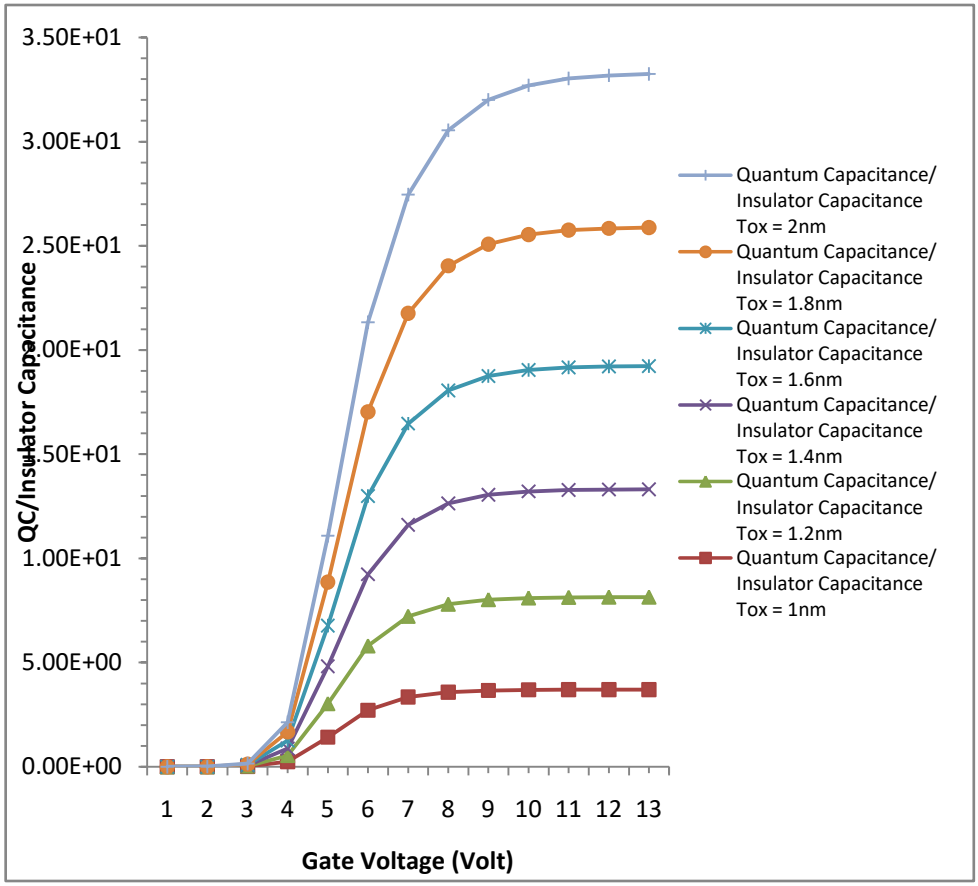

Figure 12: Graph of QC/IC ratio against gate voltage for different oxide thicknesses in single gate MOSFET

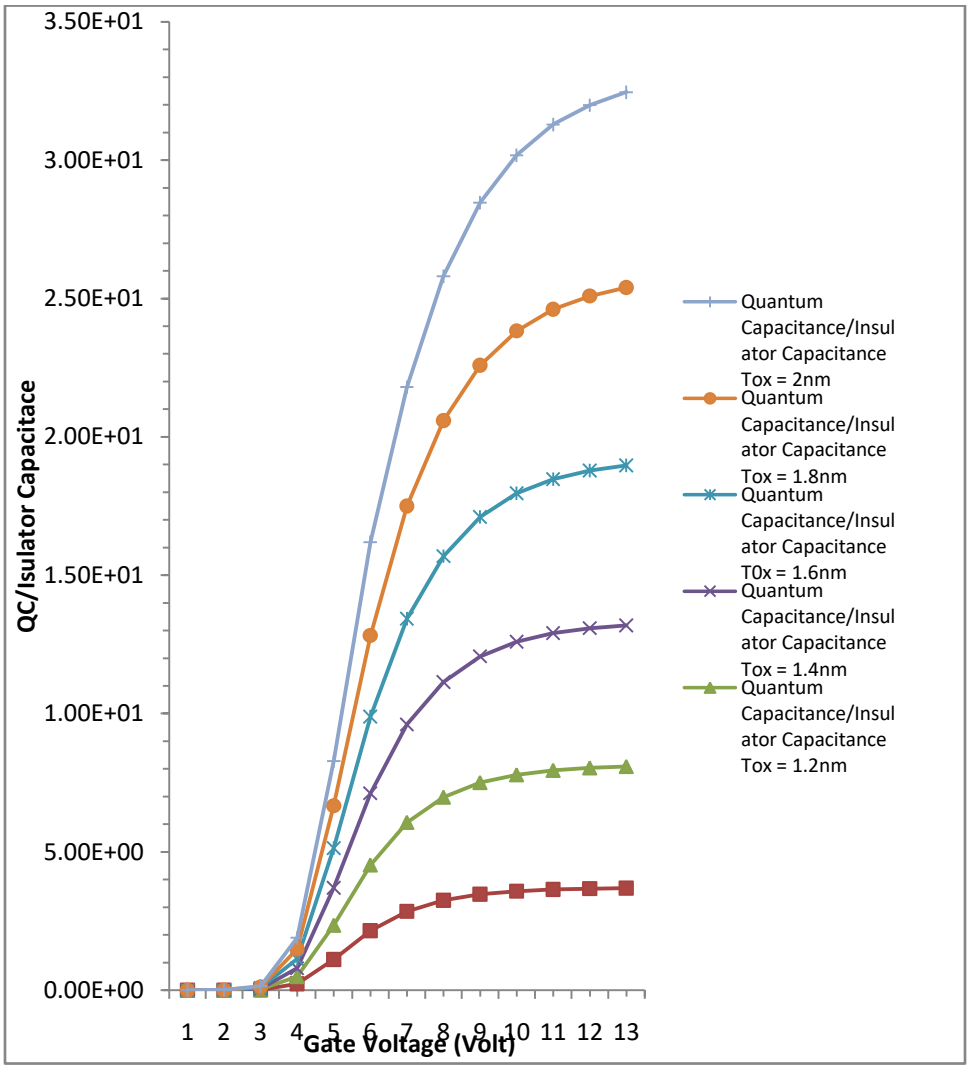

Figure 13: Graph of QC/IC ratio against gate voltage for different oxide thicknesses in double gate MOSFET

A graph of QC/Insulator capacitance ratio against gate voltage was plotted for both single gate and double gate Nano-MOSFET for all oxide thickness (1nm, 1.2nm, 1.4nm 1.6nm, 1.8nm and 2nm) as shown in Figure.12 and Figure 13.

CONCLUSION

Performance analysis of electrical properties of single gate and double gate nano-MOSFET devices was carried out using FETTOY software. The oxide thickness was varied from 1.0 nm to 2.0 nm to investigate the drain current, quantum capacitance, Gm/Id (Transconductance/Drain current) and quantum capacitance/insulator. This study concludes that double gate MOSFET device displayed improved performance over single gate due to high conductivity to minimize thermal effect, leakage current and short channel effects (SCEs).

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